Listing of the Claims:

1. (Currently Amended) A chip comprising:

a microprocessor; and

an integrated non-volatile programmable memory that stores protection data in a protection data memory portion and protected data in a protected data memory portion, wherein said protection data defines a protection level for authorizing or denying access to said protected data memory portion by said microprocessor while a program is executed, and wherein said protection data is ~~only~~ modifiable ~~so as~~ only to increase said protection level by ~~permanently~~ non-reversibly reducing access to a part of the protected data memory portion, and said protected data includes data to activate or deactivate an optional feature of the chip.

2. Canceled

3. (Previously Presented) A chip according to Claim 1, wherein said protection data includes a password, said access being authorized/denied through a password check.

4. Canceled

5. (Previously Presented) A chip according to Claim 1, wherein said optional feature is a connection to an external device for downloading a program and/or data from said external device.

6. (Previously Presented) A chip according to Claim 1, wherein said protected data includes data to activate/deactivate an external boot program for said microprocessor, said external boot program including instructions for downloading a new boot program for said microprocessor from an external memory.

7. (Previously Presented) A chip according to Claim 1, wherein said protection data includes at least one address value defining an address limit from which the data stored at said memory are protected data and access to such protected data is denied.

8. (Previously Presented) A chip according to Claim 7, wherein said protected data includes programs and data operating a conditional-access dedicated microprocessor.

9. (Currently Amended) A device that recovers a content from a media and processes said content comprising:

a connection to said media and a chip,

the chip comprising:

at least a microprocessor; and

an integrated non-volatile programmable memory that stores protection data in a protection data memory portion and protected data in a protected data memory portion, said protection data defining a protection level for authorizing or denying access to said protected data by said microprocessor while a program is executed, wherein said protection data is ~~only~~ modifiable ~~so as~~ only to increase said protection level by ~~permanently~~ non-reversibly reducing access to a part of the protected data memory portion, and wherein said protected data includes data to activate or deactivate an optional feature of the chip.

10. (Previously Presented) A device as claimed in Claim 9, wherein the device is intended to process encrypted video/audio data.

11. (Currently Amended) A method for protecting a chip comprising at least a microprocessor, said method comprising:

using at least an authorized access to modify a first protected data portion in a first integrated non-volatile memory,

protecting the access to said first protected data portion in said first integrated non-volatile memory by modifying a first protection data portion of the first integrated non-volatile memory in order to deny said access, wherein said protection data is ~~only~~ modifiable ~~so as~~ only to increase said protection level by ~~permanently~~ non-reversibly reducing access to a part of the first protected data memory portion, and said protected data includes data to ~~activate/deactivate~~ activate or deactivate an optional feature of the chip.

12. (Previously Presented) A chip according to Claim 1 further comprising a random logic coupled between said integrated non-volatile programmable memory and a connection bus of said microprocessor.

13. (Previously Presented) A chip according to Claim 1, wherein said microprocessor is a processor having a MIPS instruction set.

14. (Previously Presented) The method of claim 11 wherein the first protected data portion comprises a set of conditional access microprocessor instructions and the first protection data portion comprises a first set of address data associated with the set of conditional access microprocessor instructions that is readable by the microprocessor.

15. (Currently Amended) The method of claim 14 wherein the access to the part of the first protected data memory portion is ~~permanently~~ non-reversibly reduced by modification of the first set of address data.

16. (Currently Amended) The method of claim 15 further comprising:

using at least a second authorized access to modify a second protected data portion in the first integrated non-volatile memory, wherein the second protected data portion comprises a set of conditional access microprocessor

data and a deciphering key, with the deciphering key allocated to a lowest address of the second protected data portion;

protecting the access to the second protected data portion in the first integrated non-volatile memory by modifying a second protection data portion of the first integrated non-volatile memory in order to deny access to the second protected data portion, wherein said second protection data portion is ~~only~~ modifiable ~~so as~~ only to increase said protection level by ~~permanently~~ non-reversibly reducing access to at least a part of the second protected data memory portion.

17. (Currently Amended) The method of claim ~~17~~ 16 wherein the second protection data portion comprises a second address data that is the lowest address in the second protected data portion readable by the microprocessor, wherein the set of address data is initially associated with the lowest address of the second protected data portion; and

wherein the second protection data portion is ~~only~~ modifiable ~~so as~~ only to increase said protection level by increasing the value of the second address data.